The following listing of claims will replace all prior versions, and listings, of claims in the present application.

LISTING OF CLAIMS:

Claim 1 (Currently Amended) A method of forming a metal silicide on a surface of a Si-containing material comprising the steps of:

providing a structure comprising a metal-containing silicon alloy layer over a Si-containing material;

subjecting said structure to a first anneal which comprises a first thermal cycle which is performed at a first temperature of less than about 350°C that enhances uni-directional diffusion of said metal into said Si-containing material thereby forming an amorphous metal-containing silicide and a second thermal cycle which is performed at a second temperature that converts the amorphous metal-containing silicide into a crystallized metal rich silicide that is substantially non-etchable as compared to the metal-containing silicon alloy layer;

removing any unreacted metal-containing silicon alloy layer from the structure; and

subjecting said structure to a second anneal at a third temperature that converts said crystallized metal rich silicide into a metal silicide phase that is in its lowest resistance phase.

Claim 2 (Original) The method of Claim 1 wherein said metal-containing silicon alloy layer is formed by deposition of the alloy layer or by first depositing a refractory metal to form a metal layer and then doping the refractory metal layer with silicon.

Claim 3 (Original) The method of Claim 1 further comprising forming an optional barrier layer over said metal-containing silicon alloy layer prior to said first anneal, wherein said optional barrier layer is removed in said removing of the unreacted metal-containing silicon alloy layer.

Claim 4 (Original) The method of Claim 1 wherein said metal-containing silicon alloy layer further comprises at least one additive selected from the group consisting of C, Al, Ge, Sc, Ti, V, Cr, Mn, Fe, Cu, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir, Pt, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu and mixtures thereof.

Claim 5 (Original) The method of Claim 1 wherein said metal-containing silicon alloy layer comprises less than about 30 atomic % Si.

Claim 6 (Original) The method of Claim 1 wherein said metal-containing silicon alloy comprises Ni, Co or alloys thereof.

Claim 7 (Original) The method of Claim 1 wherein said first temperature is less than said second temperature.

Claim 8 (Cancelled)

Claim 9 (Original) The method of Claim 1 wherein said first thermal cycle is performed for a time period from about 30 seconds to about 120 seconds.

Claim 10 (Original) The method of Claim 7 wherein said second temperature is less than about 450°C, yet greater than the first temperature.

Claim 11 (Original) The method of Claim 10 wherein said second temperature is from about 350° to about 400°C.

Claim 12 (Original) The method of Claim 1 wherein said second thermal cycle is performed for a time period from about 10 seconds to about 30 seconds.

Claim 13 (Original) The method of Claim 1 wherein said removing comprises a wet etch process in which a chemical etchant is employed.

Claim 14 (Original) The method of Claim 1 wherein said third temperature is from about 700° to about 900°C and said second anneal is carried out for a time period from about 300 seconds or less.

Claim 15 (Currently Amended) A method of forming a cobalt disilicide on a surface of a Si-containing material comprising the steps of:

providing a structure comprising a cobalt (Co) silicon alloy layer over a Si-containing material;

subjecting said structure to a first anneal which comprises a first thermal cycle which is performed at a first temperature of less than about 350°C that enhances uni-directional diffusion of Co into said Si-containing material thereby forming an amorphous Co silicide and a second thermal

cycle which is performed at a second temperature that converts the amorphous Co silicide into a crystallized Co rich silicide that is substantially non-etchable as compared to the Co silicon alloy layer;

removing any non-reacted Co silicon alloy layer from the structure; and

subjecting said structure to a second anneal at a third temperature that converts said crystallized Co rich silicide into Co disilicide.

Claim 16 (Original) The method of Claim 15 wherein said Co silicon alloy layer is formed by deposition of the alloy layer or by first depositing Co to form a metal layer and then doping the metal layer with silicon.

Claim 17 (Original) The method of Claim 15 further comprising forming an optional barrier layer over said Co silicon alloy layer prior to said first anneal, wherein said optional barrier layer is removed in said removing of the Co silicon alloy layer.

Claim 18 (Original) The method of Claim 15 wherein said Co silicon alloy layer further comprises at least one additive selected from the group consisting of C, Al, Ge, Sc, Ti, V, Cr, Mn, Fe, Cu, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir, Pt, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu and mixtures thereof.

Claim 19 (Original) The method of Claim 15 wherein said Co silicon alloy layer comprises less than about 30 atomic % Si.

Claim 20 (Cancelled)

Claim 21 (Original) The method of Claim 20 wherein said first temperature is from about 270° to about 325°C.

Claim 22 (Original) The method of Claim 15 wherein said second temperature is less than about 450°C, yet greater than the first temperature.

Claim 23 (Original) The method of Claim 22 wherein said second temperature is from about 350° to about 400°C.

Claim 24 (Original) The method of Claim 15 wherein said removing comprises a wet etch process in which a chemical etchant is employed.

Claim 25 (Original) The method of Claim 15 wherein said third temperature is from about 700° to about 900°C and said second anneal is carried out for a time period from about 300 seconds or less.

Claim 26 (Withdrawn) A semiconductor structure comprising

a silicon-containing material having regions in which a metal silicide is located thereon, said metal silicide is in its lowest resistance phase and has a thickness from about 14 to about 25 nm,

whereby said metal silicide is not located atop isolation trench regions thereby reducing leakage within the structure.

Claim 27 (Withdrawn) The semiconductor structure of Claim 26 wherein said metal silicide is cobalt disilicide or nickel monosilicide.

Claim 28 (Withdrawn) The semiconductor structure of Claim 26 wherein said metal silicide is continuous containing no embedded oxide therein.

Claim 29 (Withdrawn) The semiconductor structure of Claim 26 wherein said Si-containing material comprises a substrate, a gate electrode or both.

Claim 30 (Withdrawn) The semiconductor structure of Claim 26 wherein said Si-containing material comprises single crystal Si, polycrystalline Si, SiGe, amorphous Si, silicon-on-insulator (SOI) or silicon germanium-on-insulator (SGOI).